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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,347	02/06/2004	Toshihiro Sawamoto	9319S-000665	5263

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,347	SAWAMOTO ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 10-13* is/are rejected.

7)☒ Claim(s) *3-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Applicants' amendment filed June 26, 2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 10-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Rinne (US 2004/0124520 A1).

In regard to claims 1, Rinne teaches a semiconductor device, comprising: a first semiconductor package 10a in which a first semiconductor chip (inside 10a) (page 4, paragraphs [0041]-[0042]) is mounted; a second semiconductor package 10b in which at least one semiconductor chip (inside 10b) (page 4, paragraphs [0041]-[0042]) is mounted and is supported on the first semiconductor package 10a such that ends of the second semiconductor package 10b are arranged above the first semiconductor chip (inside 10a) (page 4, paragraphs [0041]-[0042]); and a third semiconductor package 10c that is supported on the first semiconductor package 10a such that ends of the

third semiconductor package 10c are arranged above the first semiconductor chip (inside 10a) (page 4, paragraphs [0041]-[0042]) (Figure 5, pages 4-5, paragraphs [0039]-[0050]).

In regard to claim 10, Rinne teaches a semiconductor device, comprising: a first semiconductor package 10a in which a first semiconductor chip (inside 10a) (page 4, paragraphs [0041]-[0042]) is mounted; a second semiconductor chip (inside 10b) (page 4, paragraphs [0041]-[0042]) that is supported on the first semiconductor package 10a such that ends of the second semiconductor chip (inside 10b) (page 4, paragraphs [0041]-[0042]) are arranged above the first semiconductor chip (inside 10a) (page 4, paragraphs [0041]-[0042]); and a third semiconductor chip (inside 10c) (page 4, paragraphs [0041]-[0042]) that is supported on the first semiconductor package 10a such that ends of the third semiconductor chip (inside 10c) (page 4, paragraphs [0041]-[0042]) are arranged above the first semiconductor chip (inside 10a) (page 4, paragraphs [0041]-[0042]) (Figure 5, pages 4-5, paragraphs [0039]-[0050]).

In regard to claim 11, it is inherent that the second semiconductor chip (inside 10b) (page 4, paragraphs [0041]-[0042]) includes a three-dimensional mounting structure 50c because the structure occupies all planes.

In regard to claim 12, Rinne teaches an electronic device, comprising: a first package 10a in which an electronic component (inside 10a) (page 4, paragraphs [0041]-[0042]) is mounted; a second package 10b that is supported on the first semiconductor package 10a such that ends of the second package 10b are arranged above the electronic component (inside 10a) (page 4, paragraphs [0041]-[0042]); and a third

package 10c that is supported on the first package 10a such that ends of the third package 10c are arranged above the electronic component (inside 10a) (page 4, paragraphs [0041]-[0042]) (Figure 5, pages 4-5, paragraphs [0039]-[0050]).

In regard to claim 13, Rinne teaches an electronic equipment, comprising: a first semiconductor package 10a in which a semiconductor chip (inside 10a) (page 4, paragraphs [0041]-[0042]) is mounted; a second semiconductor package 10b that is supported on the first semiconductor package 10a such that ends of the second semiconductor package 10b are arranged above the semiconductor chip (inside 10a) (page 4, paragraphs [0041]-[0042]); a motherboard 210 on which the second semiconductor package 10b is mounted; and a third semiconductor package 10c that is supported on the first semiconductor package 10a such that ends of the third semiconductor package 10c are arranged above the semiconductor chip (inside 10a) (page 4, paragraphs [0041]-[0042]) (Figure 5, pages 4-5, paragraphs [0039]-[0050]).

Allowable Subject Matter

Claims 3-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1 and 10-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor devices:

Blackshear et al. (US 2003/0137041 A1)

Moshayedi (US 2004/0212071 A1)

Yagi et al. (US 2004/0104469 A1)

Yang et al. (US 2003/0141582 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IMS
September 16, 2006

IDA M. SOWARD
PRIMARY EXAMINER